

Claims

What is claimed is:

- 1 1. A method for implementing dynamic Virtual Lane (VL) buffer reconfiguration in a channel adapter comprising the steps of:
 - 2 providing a first register for communicating an adapter buffer size and allocation capability for the channel adapter;
 - 3 providing at least one second register for communicating a current port buffer size; one said second register associated with each physical port of the channel adapter;
 - 4 providing a plurality of third registers for communicating a current VL buffer size; one said third register associated with each VL of each said physical port of the channel adapter; and
 - 5 utilizing said second register for receiving change requests for adjusting said current port buffer size for an associated physical port; and
 - 6 utilizing said third register for receiving change requests for adjusting said current VL buffer size for an associated VL.
- 1 2. A method for implementing dynamic Virtual Lane (VL) buffer reconfiguration as recited in claim 1 wherein said first register includes predefined fields for storing said adapter buffer size, a flexibly allocated buffer space for the channel adapter, and an allocation unit for buffer allocation.
- 1 3. A method for implementing dynamic Virtual Lane (VL) buffer reconfiguration as recited in claim 1 wherein each said second register includes predefined fields for storing said current port buffer size, a fixed port buffer space and a requested port buffer size.
- 1 4. A method for implementing dynamic Virtual Lane (VL) buffer reconfiguration as recited in claim 1 wherein each said third register includes predefined fields for storing said current VL buffer size, a fixed VL buffer space and a requested VL buffer size.

1 5. A method for implementing dynamic Virtual Lane (VL) buffer
2 reconfiguration as recited in claim 1 wherein utilizing said second register for
3 receiving change requests for adjusting said current port buffer size for said
4 associated physical port includes the steps of utilizing a hypervisor for writing
5 said change request to a requested port buffer field of said second register
6 for adjusting said current port buffer size for said associated physical port.

1 6. A method for implementing dynamic Virtual Lane (VL) buffer
2 reconfiguration as recited in claim 1 wherein utilizing third register for
3 receiving change requests for adjusting said current VL buffer size for said
4 associated VL includes the steps of utilizing a hypervisor for writing said
5 change request to a requested VL buffer field of said third register for
6 adjusting said current port buffer size for said associated physical port.

1 7. A method for implementing dynamic Virtual Lane (VL) buffer
2 reconfiguration as recited in claim 1 further includes providing a plurality of
3 change and status registers for communicating VL change and status
4 values; one said change and status register associated with each said VL of
5 each said physical port of the channel adapter register.

1 8. A method for implementing dynamic Virtual Lane (VL) buffer
2 reconfiguration as recited in claim 1 includes providing a hypervisor for
3 monitoring buffer resources, and using said hypervisor for writing change
4 requests to respective ones of each said second register and said third
5 registers.

1 9. A method for implementing dynamic Virtual Lane (VL) buffer
2 reconfiguration as recited in claim 1 further includes providing channel
3 adapter hardware for managing allocation of buffer space responsive to said
4 change requests written by said hypervisor.

1 10. A method for implementing dynamic Virtual Lane (VL) buffer
2 reconfiguration as recited in claim 1 wherein providing said hypervisor for
3 monitoring buffer resources includes providing at least one register for
4 storing VL buffer usage statistics; and said hypervisor periodically polling
5 said at least one register for storing VL buffer usage statistics.

1 11. Apparatus for implementing dynamic Virtual Lane (VL) buffer
2 reconfiguration comprising:
3 a first register for communicating an adapter buffer size and allocation
4 capability for a channel adapter;
5 at least one second register for communicating a current port buffer
6 size; one said second register associated with each physical port of the
7 channel adapter;
8 a plurality of third registers for communicating a current VL buffer
9 size; one said third register associated with each VL of each said physical
10 port of the channel adapter;
11 a hypervisor for writing change requests to said second register for
12 adjusting said current port buffer size for an associated physical port; and
13 said hypervisor for writing change requests to said third register for
14 adjusting said current VL buffer size for an associated VL; and
15 channel adapter hardware for managing allocation of buffer space
16 responsive to said change requests written by said hypervisor.

1 12. Apparatus for implementing dynamic Virtual Lane (VL) buffer
2 reconfiguration as recited in claim 11 wherein said first register includes
3 predefined fields for storing said adapter buffer size, a flexibly allocated
4 buffer space for the channel adapter, and an allocation unit used for buffer
5 allocation.

1 13. Apparatus for implementing dynamic Virtual Lane (VL) buffer
2 reconfiguration as recited in claim 11 wherein each said second register
3 includes predefined fields for storing said current port buffer size, a fixed port
4 buffer space and a requested port buffer size; said hypervisor writes said
5 change requests to said requested port buffer size field.

1 14. Apparatus for implementing dynamic Virtual Lane (VL) buffer
2 reconfiguration as recited in claim 11 wherein said channel adapter
3 hardware includes buffer management state machine hardware.

1 15. Apparatus for implementing dynamic Virtual Lane (VL) buffer
2 reconfiguration as recited in claim 11 wherein each said third register
3 includes predefined fields for storing said current VL buffer size, a fixed VL
4 buffer space and a requested VL buffer size; said hypervisor writes said
5 change requests to said requested VL buffer size field.

1 16. Apparatus for implementing dynamic Virtual Lane (VL) buffer
2 reconfiguration as recited in claim 11 includes at least one register storing
3 VL buffer usage statistics; and said hypervisor for monitoring buffer
4 resources and periodically polling said at least one register storing VL buffer
5 usage statistics.

1 17. A computer program product for implementing dynamic Virtual
2 Lane (VL) buffer reconfiguration in a channel adapter of a system area
3 network, said computer program product including a plurality of computer
4 executable instructions stored on a computer readable medium, wherein
5 said instructions, when executed by the channel adapter, cause the channel
6 adapter to perform the steps of:

7 communicating an adapter buffer size and allocation capability for the
8 channel adapter using a first register;

9 communicating a current port buffer size using a second register; one
10 said second register associated with each physical port of the channel
11 adapter;

12 communicating a current VL buffer size using a third register; one said
13 third register associated with each VL of each said physical port of the
14 channel adapter; and

15 writing a change request to one said second register for adjusting said
16 current port buffer size for said associated physical port; and

17 writing a change request to one said third register for adjusting said
18 current VL buffer size for said associated VL.

1 18. A computer program product as recited in claim 17 wherein
2 said instructions, when executed by the channel adapter, cause the channel
3 adapter to perform the steps of: monitoring buffer resources by periodically
4 polling a register storing VL buffer usage statistics.

1 19. A computer program product as recited in claim 17 wherein
2 said instructions, when executed by the channel adapter, cause the channel
3 adapter to perform the steps of: writing said change requests responsive to
4 monitoring buffer resources.